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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,412	04/19/2006	Koichi Terashima	040373-0382	3430
22428	7590	10/08/2009	EXAMINER	
FOLEY AND LARDNER LLP			WILSON, ALLAN R	
SUITE 500				
3000 K STREET NW			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20007			2815	
			MAIL DATE	DELIVERY MODE
			10/08/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,412	TERASHIMA ET AL.	
	Examiner	Art Unit	
	ALLAN R. WILSON	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 July 2009.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
 4a) Of the above claim(s) 2-5,8-19 and 22 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,6,7,20,21 and 23 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Response to Arguments

Applicant's arguments, see pages 8-9, filed July 14, 2009, with respect to the rejection(s) of claim(s) 1, 6, 7, 20 and 21 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yeo et al. Due to a printing error, Hareland et al. was incorrectly listed as the primary reference. The Examiner regrets any inconvenience.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 6, 7, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,867,433 to Yoe et al. (hereinafter "Yoe") in view of US Patent Application Publication No. 2002/0011612 to Hieda (of record).

Regarding claim 1, Yoe illustrates in at least figures 3c-8c with the associated text:

A semiconductor device comprising a protruding semiconductor region 155 formed on a substrate (152 and 158), a protruding source/drain region 172/174 sandwiching the semiconductor region and a gate electrode 160 formed at least on lateral sides of the semiconductor region via an insulating film 164 (best seen in figs. 3c and 3d),

wherein the source/drain region has a slope (curved side) in which at least the largest width is larger than a width of the semiconductor region and width continuously increases from the uppermost side to the substrate side in the source/drain region.

Yoe does not show a silicide film is formed on the surface of the slope. Hieda discloses in paragraph [0219] a silicide film is formed on the surface of the source/drain region 17. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a silicide film is formed on the surface of the source/drain region slope of Yoe. The motivation for doing this is to decrease the specific resistance (Hieda [0219]).

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Regarding claim 6, Hieda discloses in paragraph [0219] the source/drain region(s) is composed from the slope(s) having a silicide film on its surface. It would have been obvious to one of ordinary skill in the art to have the whole of the source/drain region(s) covered with a silicide to provide maximum decrease in the specific resistance.

Regarding claim 7, Yoe illustrates in figs. 3c and 3d a width of the slope(s) in the source/drain region(s) 155 increases from the uppermost side to the substrate side (152 and 158) in a constant rate.

Regarding claim 20, Yoe discloses in col. 6, lines 25-30, the substrate 152 is an insulating film layer (buried insulator), on which the protruding semiconductor region(s) (154 and 155) and the protruding source/drain region(s) (172 and 174) are formed.

Regarding claim 21, Yoe illustrates in figs. 3c-8b (best seen in fig. 7) the substrate (152 and 158) is an interlayer insulating film (The buried insulator and isolation region are between the silicon substrate and inherent metal layers for connecting the device. Therefore, they are interlayer insulating films.), and the protruding semiconductor region(s) 155 and the protruding source/drain region(s) (172 and 174) are parts of the semiconductor layer formed under the interlayer insulating film (below the “surface”), which penetrates the interlayer insulating film and protrudes above the interlayer insulating film.

Regarding claim 23, Yoe illustrates in fig. 5 the lateral sides (sides of 160) are perpendicular to a substrate plane of the substrate 152.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is 571-272-1738. Examiner Wilson can normally be reached 7:00-3:30 Monday-Friday (off first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Allan R. Wilson/
Primary Examiner, Art Unit 2815